



**RECEIVED
CENTRAL FAX CENTER**

MAR 20 2006

**North America
Intellectual Property Corporation**

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562

FAX: 806-498-6673

e-mail: winstonhsu@naipo.com

Customer No.: 27765

**Fax To: WILLIAMS, ALEXANDER O
Art Unit: 2826**

**Tel.: (571) 272-1924
Fax: (571) 273-8300**

From: Winston Hsu, Registration No. 41,526

Serial No.: 10/695,630

Attorney Docket No.: MEGP0005USA4

**Subject: Supplemental Amendment And Response to the
Office Action mailed on 12/15/2005**

Total Pages: 19 pages (including cover page)

Winston Hsu 03/20/2006

MEGP0005USA4_A3_2

PTO/SB/21 (09-04)

Approved for use through 07/31/2006. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/695,630	
	Filing Date	10/27/2003	
	First Named Inventor	Shih-Hsiung Lin	
	Art Unit	2826	
	Examiner Name	WILLIAMS, ALEXANDER O	
Total Number of Pages in This Submission	18	Attorney Docket Number	MEGP0005USA4

**RECEIVED
CENTRAL FAX CENTER**
MAR 20 2006

ENCLOSURES (Check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached <input checked="" type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation <input type="checkbox"/> Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input type="checkbox"/> Other Enclosure(s) (please identify below):
Remarks: _____		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	North America Intellectual Property Corporation		
Signature	<i>Winston Hsu</i>		
Printed name	Winston Hsu		
Date	3/20/2006	Reg. No.	41,526

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:			
Signature	<i>Janice Chen</i>		
Typed or printed name	Janice Chen	Date	3/20/2006

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

RECEIVED
CENTRAL FAX CENTER

MAR 20 2006

PTO/SB/17 (12-04v2)

Approved for use through 07/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

Effective on 12/08/2004.

Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005☒ Applicant claims small entity status. See 37 CFR 1.27TOTAL AMOUNT OF PAYMENT (\$)**0.00****Complete if Known**

Application Number	10/695,630
Filing Date	10/27/2003
First Named Inventor	Shih-Hsiung Lin
Examiner Name	WILLIAMS, ALEXANDER O
Art Unit	2826
Attorney Docket No.	MEGP0005USA4

METHOD OF PAYMENT (check all that apply)☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____☒ Deposit Account Deposit Account Number: **50-3105** Deposit Account Name: **North America Intellectual Property Corporation**

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee
☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION**1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Small Entity	Fee (\$)	Small Entity	Fee (\$)	Small Entity	Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee (\$)	Fee Paid (\$)	Multiple Dependent Claims
- 20 or HP = _____ x _____ = _____				Fee (\$) Fee Paid (\$)

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee (\$)	Fee Paid (\$)
- 3 or HP = _____ x _____ = _____			

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
- 100 = _____ / 50 _____ (round up to a whole number) x _____ = _____				

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge): _____

Fees Paid (\$)**SUBMITTED BY**

Signature	<i>Winston Hsu</i>	Registration No. (Attorney/Agent)	41,526	Telephone	3027291562
Name (Print/Type)	Winston Hsu	Date	3/20/2006		

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**RECEIVED
CENTRAL FAX CENTER****MAR 20 2006****IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**In Re Application of:)
)5 Applicants : SHIH-HSIUNG LIN ET AL.) Examiner: WILLIAMS,
ALEXANDER OSerial No.: 10/695,630) Art Unit: 2826
)10 Filed: 10/27/2003)
)

For: CHIP PACKAGE WITH MULTIPLE CHIPS

15

SUPPLEMENTAL AMENDMENT AND RESPONSE TO OFFICE ACTION

Commissioner for Patents

20 P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following response contains marked changes to the claims and specification.

25 In the amendment previously filed on March 15, 2006, only clean versions of the claims and specification were provided, and no marked changes were shown.

The Office Action mailed December 15, 2005 has been carefully considered. In response thereto, please enter the following amendments and consider the following

30 remarks.

AMENDMENTS

IN THE SPECIFICATION

Please replace the title with the following title:

5

CHIP PACKAGE WITH MULTIPLE CHIPS CONNECTED BY BUMPS

Please amend the following paragraph under the section labeled,
CROSS-REFERENCE TO RELATED REFERENCE.

10

~~This application is a continuation-in-part application of application serial no. 09/798,654, filed on March 05, 2001, now pending. This application is a continuation-in-part application of application serial no. 10/055,580, filed on January 22, 2002, now pending.~~ This application claims the priority benefit of Taiwan
15 application serial no. 91125126, filed on October 25, 2002. This application is related to application No. 09/798,654 filed on Mar. 5, 2001, now Pat. No. 6,818,545; and related to application No. 10/935,451 filed on Sep. 7, 2004, now pending; and related to application No. 09/953,525 filed on Sep. 17, 2001, now Pat. No. 6,642,136; and related to application No. 10/638,454 filed on Aug. 11, 2003, now Pat. No.
20 6,917,119; and related to application No. 11/120,234 filed on May 2, 2005, now pending; and related to application No. 09/837,007 filed on Apr. 18, 2001, now pending; and related to application No. 10/055,580 filed on Jan. 22, 2002, now pending; and related to application No. 10/174,357 filed on Jun. 17, 2002, now Pat. No. 6,784,087; and related to application No. 10/874,704 filed on Oct. 27, 2003, now
25 pending; and related to application No. 11/123,328 filed on May 6, 2005, now pending, all assigned to a common assignee.

In The Claims:

Claims 1-74 (canceled)

- 5 75. (currently amended) A multi-chip structure comprising:
a first chip comprising a pad comprising a copper layer and a nickel layer over
said copper layer;
a second chip; and
a ~~conductive pillar on the first chip, wherein said conductive pillar has a height~~
10 ~~greater than 3 microns; and~~
a tin-containing material connecting said pad ~~conductive pillar~~ to said second
chip.

Claims 76-77 (canceled)

- 15 78. (currently amended) The structure of Claim 75, wherein said pad further
~~conductive pillar~~ comprises a gold layer over said nickel layer.

- 20 79. (currently amended) The structure of Claim 75, wherein said tin-containing
bump ~~conductive pillar further~~ comprises copper, tin.

80. (currently amended) The structure of Claim 75 further comprising a wire
wirebonded formed by a wirebonding process and connected to said first chip.

- 25 81. (previously presented) The structure of Claim 75, wherein said tin-containing
material further comprises lead.

82. (previously presented) The structure of Claim 75, wherein said tin-containing
material further comprises silver.

- 30 83. (currently amended) A multi-chip structure, comprising:
a first chip comprising:

a semiconductor substrate comprising multiple MOS devices,

a metallization structure ~~an interconnection layer~~ over said semiconductor substrate,

5 ~~a first pad over said semiconductor substrate~~, a passivation layer over said metallization structure, ~~interconnection layer~~, an opening in said passivation layer exposing a top surface of a said first pad of said metallization structure, and

10 ~~a second pad over said passivation layer, wherein said second pad is connected to said top surface of said first pad, wherein said second pad comprising a copper layer and a nickel layer over said copper layer; and has a position different from that of said first pad from a top view;~~

~~a conductive pillar on said second pad, wherein said conductive pillar has a height greater than 3 microns;~~

a second chip over said first chip; and

15 a tin-containing material connecting said second pad ~~conductive pillar~~ to said second chip.

Claims 84-85 (canceled)

20 86. (currently amended) The structure of Claim 83, wherein said second pad further ~~conductive pillar~~ comprises a gold layer over said nickel layer.

25 87. (currently amended) The structure of Claim 83, wherein said tin-containing material further ~~conductive pillar~~ comprises copper. ~~tin.~~

88. (currently amended) The structure of Claim 83, wherein said second pad further comprises a gold layer under said copper layer, wherein said gold layer has a thickness of greater than 1 micron.

30 89. (previously presented) The structure of Claim 83, wherein said second pad comprises an electroplated metal.

Claims 90 (canceled)

91. (currently amended) The structure of Claim 83 further comprising a wire wirebonded ~~formed by a wirebonding process and connected~~ to said first chip.

5

92. (previously presented) The structure of Claim 83, wherein said tin-containing material further comprises lead.

93. (previously presented) The structure of Claim 83, wherein said tin-containing material further comprises silver.

10

94. (currently amended) A multi-chip structure, comprising:

a first chip comprising:

a semiconductor substrate comprising multiple MOS devices,

15

a metallization structure ~~an interconnection layer~~ over said semiconductor substrate,

~~a first pad over said semiconductor substrate~~, a passivation layer over said metallization structure, ~~interconnection layer~~, an opening in said passivation layer exposing ~~said~~ a first pad of said metallization structure,

20

a trace over said passivation layer, and

~~a second pad over said passivation layer, wherein said second pad is connected to said first pad through said trace, wherein said second pad comprises a copper layer and a nickel layer over said copper layer, and has a position different from that of said first pad from a top view;~~

25

a second chip over said first chip; and

a tin-containing material ~~bump~~ connecting said second pad to said second chip.

Claims 95-96 (canceled)

97. (currently amended) The structure of Claim 94, wherein said second pad ~~further bump~~ comprises a gold layer over said nickel layer.

30

98. (currently amended) The structure of Claim 94, wherein said tin-containing material bump further comprises copper. tin.

5 99. (currently amended) The structure of Claim 94, wherein said tin-containing material bump further comprises lead.

100. (currently amended) The structure of Claim 94, wherein said tin-containing material bump further comprises silver.

10 101. (currently amended) The structure of Claim 94 further comprising a wire wirebonded ~~formed by a wirebonding process and connected~~ to said first chip.

102. (new) The structure of Claim 75, wherein said tin-containing material covers a top surface and a sidewall of said pad.

15 103. (new) The structure of Claim 83, wherein said tin-containing material covers a top surface and a sidewall of said second pad.

20 104. (new) The structure of Claim 83, wherein said passivation layer comprises nitride.

105. (new) The structure of Claim 94, wherein said tin-containing material covers a top surface and a sidewall of said second pad.

25 106. (new) The structure of Claim 94, wherein said trace comprises a gold layer having a thickness of greater than 1 micron.

30 107. (new) The structure of Claim 94, wherein said passivation layer comprises nitride.

REMARKS

5 This supplemental amendment contains marked changes to the claims and specification. In the amendment previously filed on March 15, 2006, only clean versions of the claims and specification were provided, and no marked changes were shown. No other changes have been made in this supplemental amendment other than to show the marked changes made to the specification and claims. Acceptance of this supplemental amendment is respectfully requested.

10 In regards to the Title, Applicants have amended the Title to "CHIP PACKAGE WITH MULTIPLE CHIPS CONNECTED BY BUMPS" to limit the focus to the claimed invention. Applicants respectfully request that this title be entered by amendment.

15 The applicant hereby withdraws a benefit for claiming prior applications. In regards to the related patents and patent applications, Applicant has provided information on related patents and patent applications relevant to the present application. Withdrawal of the disclosure being objected to is respectfully requested as the related patents and patent applications are updated.

20 Withdrawal of the drawings being objected to is respectfully requested as reference number "790" indicates wires in line 5, paragraph [0084].

25 Claims 75, 78-83, 86-89, 91-94 and 97-107 are pending; Claims 75, 78-80, 83, 86-88, 91, 94 and 97-101 are currently amended; Claims 102-107 are newly added; Claims 1-74, 76, 77, 84, 85, 90, 95 and 96 are canceled.

30 Some or all of pending claims are believed to be in condition for Allowance, and that is so requested.

Response to Claim Rejections under 35 U.S.C. 112

Withdrawal of the claim rejection under 35 U.S.C. 112, second paragraph, is respectfully requested as Claim 94 has been amended.

Response to Claim Rejections under 35 U.S.C. 102 and 103

5

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 75 and 78-82

10

=====

As currently amended, independent claim 75 is recited below:

75. A multi-chip structure comprising:

15

a first chip comprising a pad comprising a copper layer and a nickel layer over said copper layer;
a second chip; and
a tin-containing material connecting said pad to said second chip.

=====

20

==

Section I

Reconsideration of Claims 75-79 and 81-82 rejected under 35 U.S.C. 102(e) as being anticipated by US6,787,442 to Hayashida is requested in accordance with the following remarks.

25

Applicants respectfully assert that the electronic component claimed in claim 75 patentably distinguishes over the citation by Hayashida (US6,787,442).

30

Hayashida teaches that a circuitry component comprises a chip 9 and a module substrate 11 connected by multiple bumps 6. ~ See FIGS. 3 and 6 ~ Applicants respectfully traverse the Examiner opinions that Hayashida's module substrate 11 can

be considered as a chip. ~See the third paragraph, page 5, in the latest office action mailed Dec. 15, 2005~ Those skilled in the art should not typically think a module substrate can be deemed as a chip. A chip definitely has one or more P and N regions on a semiconductor substrate, formed for one or more active devices. Those
5 skilled in the art should not typically think a module substrate may have one or more P and N regions on a semiconductor substrate. The structure of a chip is significantly different from that of a module substrate.

Hayashida fails to teach a chip can be mounted to another chip, but teaches a
10 chip can be mounted to a module substrate. The mechanism or consideration of a tin-containing material connecting multiple chips is different from that of a tin-containing material connecting a chip to a module substrate because the structure of a chip is significantly different from that of a module substrate. The Examiner should search for the technology field of "a tin-containing material connecting
15 multiple chips" to build the prima-facie cases, but not search for the technology field of "a tin-containing material connecting a chip to a module substrate" to build the prima-facie cases.

For at least the foregoing reasons, applicants respectfully submit independent
20 claim 75 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 78-82 patently define over the prior art as well.

Section II

25 *Reconsideration of Claims 75-82 rejected under 35 U.S.C. 102(e) as being anticipated by US2003/0052409 to Matsuo et al is requested in accordance with the following remarks.*

Applicants respectfully assert that the electronic component claimed in claim 75
30 patentably distinguishes over the citation by Matsuo et al (US2003/0052409).

Matsuo et al teach that a circuitry component comprises two chips 303 and 307

connected to each other. ~ See FIG 12 ~ However, Matsuo et al fail to teach a tin-containing material can be used to connect two chips 303 and 307, as claimed in claim 75.

5 For at least the foregoing reasons, applicants respectfully submit independent claim 75 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 78-82 patently define over the prior art as well.

10 **Section III**

Reconsideration of Claims 75-82 rejected under 35 U.S.C. 102(e) as being anticipated by US6,734,556 to Shibata is requested in accordance with the following remarks.

15 Applicants respectfully assert that the electronic component claimed in claim 75 patentably distinguishes over the citation by Shibata (US6,734,556).

Shibata teaches that a circuitry component comprises two chips 1 and 2 connected by a tin-containing material 3. ~ See FIGS. 1B and 2A ~ The chip 1
20 comprises a pad, connected to the tin-containing material 3, constructed from a barrier metal layer 14 and a bump electrode 11, wherein the barrier metal layer 14 consists of a first layer made of Ti or Cr, a second layer made of W, Pt, Ag, Cu, or Ni, and a third layer made of Au, and wherein the bump electrode 11 is made of Au. ~ See FIG. 1C; lines 7-17, paragraph [0052] ~ However, Shibata fails to teach the pad may comprise
25 a structure of "a nickel layer over a copper layer", as claimed in claim 75.

For at least the foregoing reasons, applicants respectfully submit independent claim 75 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 78-82 patently define over the prior
30 art as well.

Response to Claims 83, 86-89 and 91-93

As currently amended, independent claim 83 is recited below:

5 83. A multi-chip structure, comprising:

a first chip comprising:

a semiconductor substrate comprising multiple MOS devices,

a metallization structure over said semiconductor substrate,

a passivation layer over said metallization structure, an

10 opening in said passivation layer exposing a top surface of a first pad
of said metallization structure, and

a second pad connected to said top surface of said first pad,
wherein said second pad comprising a copper layer and a nickel layer
over said copper layer;

15 a second chip over said first chip; and

a tin-containing material connecting said second pad to said second
chip.

20 **Section I**

*Reconsideration of Claims 83-90 and 92-93 rejected under 35 U.S.C. 102(e) as
being anticipated by US6,787,442 to Hayashida and of claim 91 rejected under 35
U.S.C. 103(a) as being unpatentable over US6,787,442 to Hayashida in view of
25 US6,734,556 to Shibata is requested in accordance with the following remarks.*

Applicants respectfully assert that the electronic component claimed in claim 83
patentably distinguishes over the citation by Hayashida (US6,787,442).

30 Hayashida teaches that a circuitry component comprises a chip 9 and a module
substrate 11 connected by multiple bumps 6. ~ See FIGS. 3 and 6 ~ Applicants
respectfully traverse the Examiner opinions that Hayashida's module substrate 11 can

be considered as a chip. ~See the third paragraph, page 5, in the latest office action mailed Dec. 15, 2005~ Those skilled in the art should not typically think a module substrate can be deemed as a chip. A chip definitely has one or more P and N regions on a semiconductor substrate, formed for one or more active devices. Those
5 skilled in the art should not typically think a module substrate may have one or more P and N regions on a semiconductor substrate. The structure of a chip is significantly different from that of a module substrate.

Hayashida fails to teach a chip can be mounted to another chip, but teaches a
10 chip can be mounted to a module substrate. The mechanism or consideration of a tin-containing material connecting multiple chips is different from that of a tin-containing material connecting a chip to a module substrate because the structure of a chip is significantly different from that of a module substrate. The Examiner should search for the technology field of "a tin-containing material connecting
15 multiple chips" to build the prima-facie cases, but not search for the technology field of "a tin-containing material connecting a chip to a module substrate" to build the prima-facie cases.

For at least the foregoing reasons, applicants respectfully submit independent
20 claim 83 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 86-89 and 91-93 patently define over the prior art as well.

Section II

25 *Reconsideration of Claims 83-93 rejected under 35 U.S.C. 102(e) as being anticipated by US2003/0052409 to Matsuo et al is requested in accordance with the following remarks.*

Applicants respectfully assert that the electronic component claimed in claim 83
30 patently distinguishes over the citation by Matsuo et al (US2003/0052409).

Matsuo et al teach that a circuitry component comprises two chips 303 and 307

connected to each other. ~ See FIG 12 ~ However, Matsuo et al fail to teach a tin-containing material can be used to connect two chips 303 and 307, as claimed in claim 83.

5 For at least the foregoing reasons, applicants respectfully submit independent claim 83 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 86-89 and 91-93 patently define over the prior art as well.

10 **Response to Claims 94 and 97-101**

As currently amended, independent claim 94 is recited below:

15 94. A multi-chip structure, comprising:
a first chip comprising:
a semiconductor substrate comprising multiple MOS devices,
a metallization structure over said semiconductor substrate,
a passivation layer over said metallization structure, an
20 opening in said passivation layer exposing a first pad of said metallization structure,
a trace over said passivation layer, and
a second pad connected to said first pad through said trace,
wherein said second pad comprising a copper layer and a nickel layer
25 over said copper layer;
a second chip over said first chip; and
a tin-containing material connecting said second pad to said second
chip.

30 ==

Section I

Reconsideration of Claims 94-100 rejected under 35 U.S.C. 102(e) as being anticipated by US6,787,442 to Hayashida and of claim 101 rejected under 35 U.S.C. 103(a) as being unpatentable over US6,787,442 to Hayashida in view of US6,734,556 to Shibata is requested in accordance with the following remarks.

5

Applicants respectfully assert that the electronic component claimed in claim 94 patentably distinguishes over the citation by Hayashida (US6,787,442).

Hayashida teaches that a circuitry component comprises a chip 9 and a module
10 substrate 11 connected by multiple bumps 6. ~ See FIGS. 3 and 6 ~ Applicants respectfully traverse the Examiner opinions that Hayashida's module substrate 11 can be considered as a chip. ~See the third paragraph, page 5, in the latest office action mailed Dec. 15, 2005~ Those skilled in the art should not typically think a module substrate can be deemed as a chip. A chip definitely has one or more P and N
15 regions on a semiconductor substrate, formed for one or more active devices. Those skilled in the art should not typically think a module substrate may have one or more P and N regions on a semiconductor substrate. The structure of a chip is significantly different from that of a module substrate.

20 Hayashida fails to teach a chip can be mounted to another chip, but teaches a chip can be mounted to a module substrate. The mechanism or consideration of a tin-containing material connecting multiple chips is different from that of a tin-containing material connecting a chip to a module substrate because the structure of a chip is significantly different from that of a module substrate. The Examiner
25 should search for the technology field of "a tin-containing material connecting multiple chips" to build the prima-facie cases, but not search for the technology field of "a tin-containing material connecting a chip to a module substrate" to build the prima-facie cases.

30 For at least the foregoing reasons, applicants respectfully submit independent claim 94 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 97-101 patentably define over the prior

art as well.

Section II

5 *Reconsideration of Claims 94-101 rejected under 35 U.S.C. 102(e) as being anticipated by US2003/0052409 to Matsuo et al is requested in accordance with the following remarks.*

10 Applicants respectfully assert that the electronic component claimed in claim 94 patentably distinguishes over the citation by Matsuo et al (US2003/0052409).

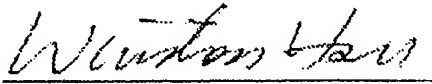
15 Matsuo et al teach that a circuitry component comprises two chips 303 and 307 connected to each other. ~ See FIG 12 ~ However, Matsuo et al fail to teach a tin-containing material can be used to connect two chips 303 and 307, as claimed in claim 94.

20 For at least the foregoing reasons, applicants respectfully submit independent claim 94 patentably distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 97-101 patentably define over the prior art as well.

25 **CONCLUSION**

For at least the foregoing reasons, it is believed that the pending claims 75, 78-83, 86-89, 91-94 and 97-107 are in proper condition for allowance.

Sincerely yours,



Date: 03/20/2006

5 Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

10

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)